Z80H CPU

Zilog

AC Characteristics

Preliminary

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SOUTH CONTINENTAL DEVICES (PTY) LTD.
P.O. Box 56420 — PINEGOWRIE 2123
Tel. 789-2400 Telex 4-24849 SA

Zilog

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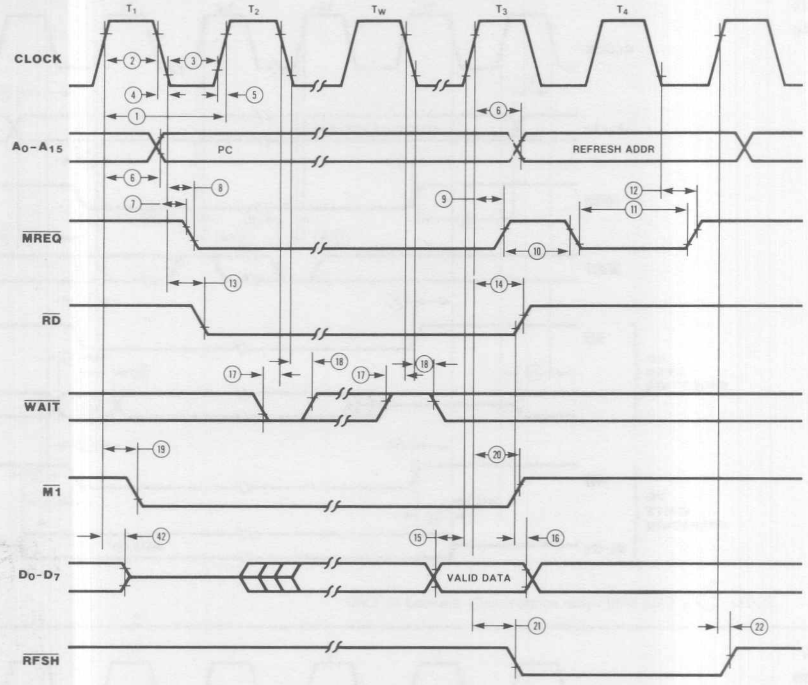
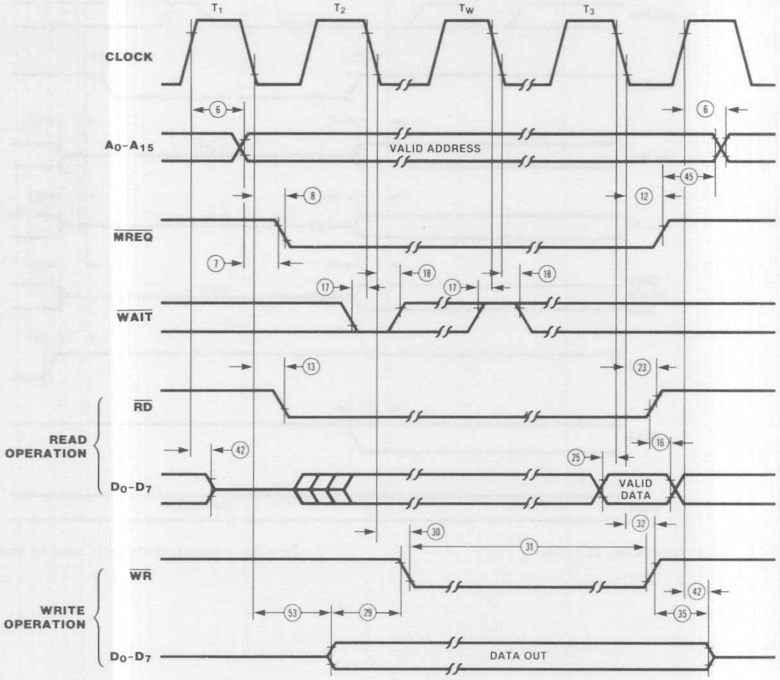
Opcode Fetch Cycle Timing

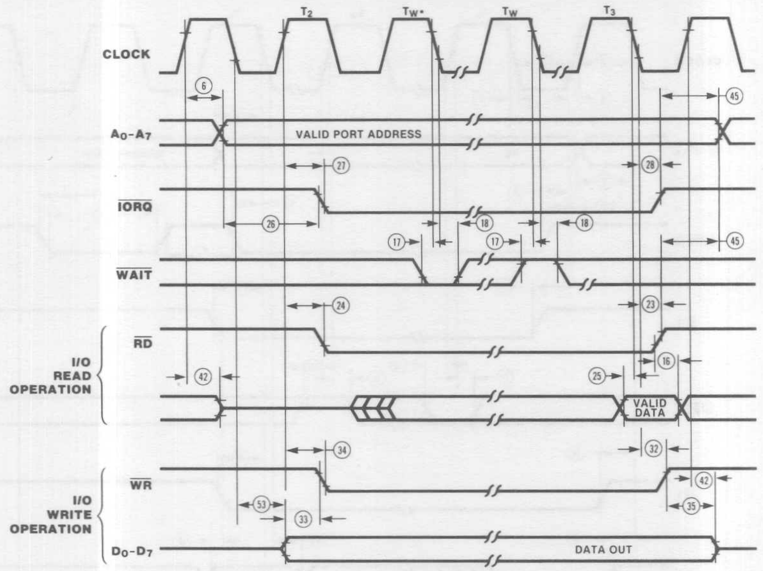


NOTE: T_W-Wait cycle added when necessary for slow ancilliary devices.

Data Memory Read/Write Cycle Timing

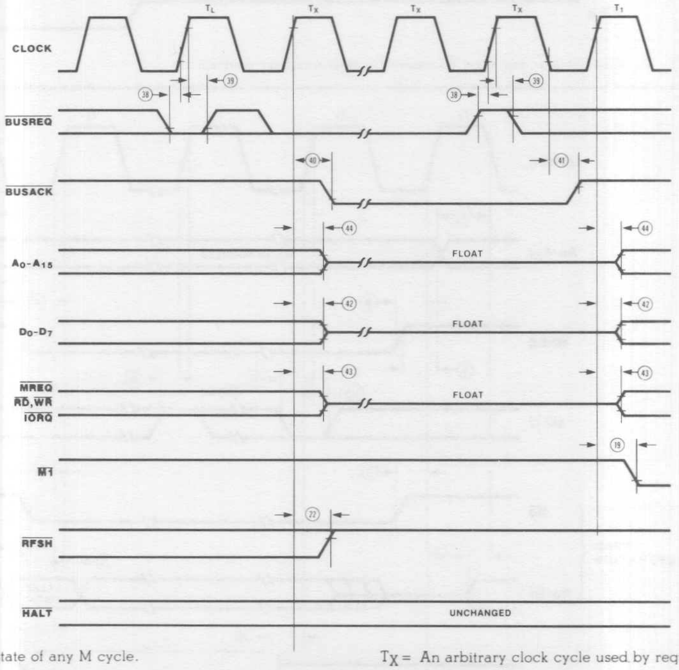


Input/Output Read & Write Timing



NOTE: T_{W^*} = One Wait cycle automatically inserted by CPU.

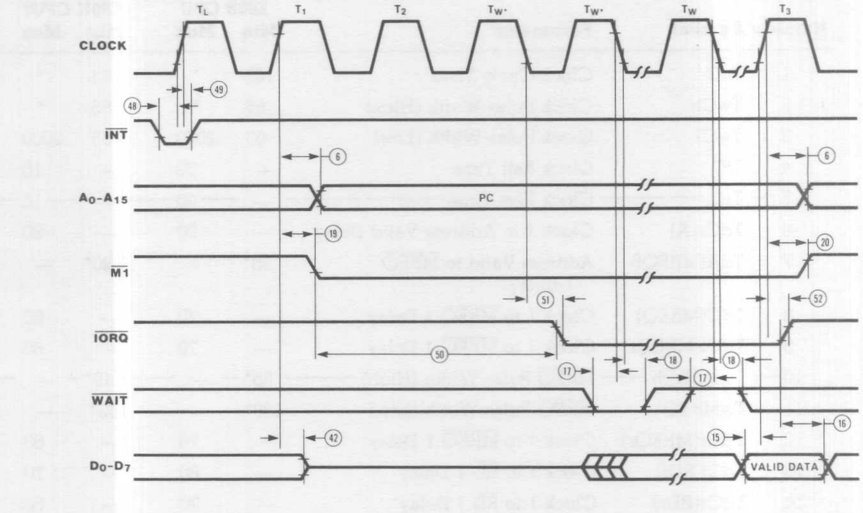
Bus Request/ Acknowledge Timing



NOTE: T_L = Last state of any M cycle.

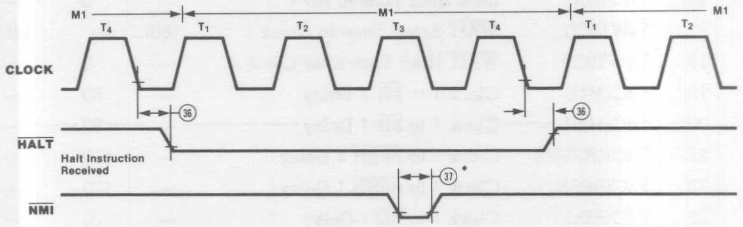
T_X = An arbitrary clock cycle used by requesting device.

Interrupt Request/ Acknowledge Timing



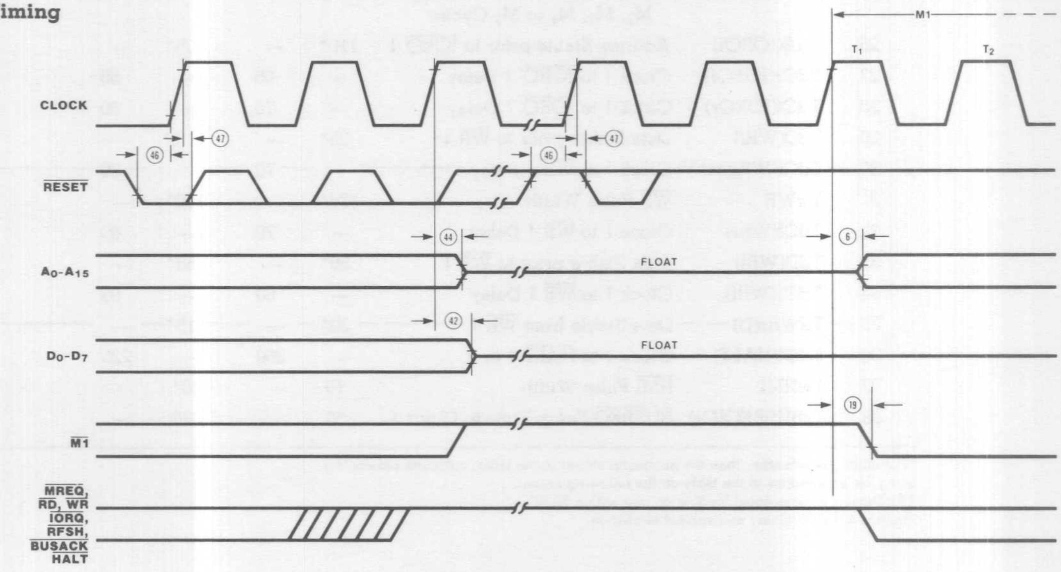
NOTE: 1) T_L = Last state of previous instruction.
2) Two Wait cycles automatically inserted by CPU(*).

Halt Acknowledge Cycle Timing



NOTE: $\overline{INT}$ will also force a Halt exit.

Reset Timing



M1
T_1
T_2
CLOCK
$\overline{RESET}$
A_0-A_{15}
D_0-D_7
$\overline{M1}$
$\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$ $\overline{IORQ}$, $\overline{RFSH}$, $\overline{BUSACK}$ $\overline{HALT}$
46
47
46
47
44
6
42
19
FLOAT
FLOAT

AC Characteristics (Continued)

Number	Symbol	Parameter	Z80B CPU		Z80H CPU†	
			Min	Max	Min	Max
1	TcC	Clock Cycle Time	165	*	125	*
2	TwCh	Clock Pulse Width (High)	65	*	55	*
3	TwCl	Clock Pulse Width (Low)	65	2000	55	2000
4	TfC	Clock Fall Time	—	20	—	10
5	TrC	Clock Rise Time	—	20	—	10
6	TdCr(A)	Clock ↑ to Address Valid Delay	—	90	—	80
7	TdA(MREQf)	Address Valid to $\overline{\text{MREQ}}$ ↓ Delay	35*	—	20*	—
8	TdC(MREQ)	Clock ↓ to $\overline{\text{MREQ}}$ ↓ Delay	—	70	—	60
9	TdCf(MREQr)	Clock ↓ to $\overline{\text{MREQ}}$ ↑ Delay	—	70	—	60
10	TwMREQh	$\overline{\text{MREQ}}$ Pulse Width (High)	65*	—	45*	—
11	TwMREQl	$\overline{\text{MREQ}}$ Pulse Width (Low)	135*	—	100*	—
12	TdCr(MREQr)	Clock ↓ to $\overline{\text{MREQ}}$ ↑ Delay	—	70	—	60
13	TdCf(RDf)	Clock ↓ to $\overline{\text{RD}}$ ↓ Delay	—	80	—	70
14	TdCr(RDr)	Clock ↑ to $\overline{\text{RD}}$ ↑ Delay	—	70	—	60
15	TsD(Cr)	Data Setup Time to Clock ↑	30	—	25	—
16	ThD(RDr)	Data Hold Time to $\overline{\text{RD}}$ ↑	—	0	—	0
17	TsWT(Cf)	$\overline{\text{WAIT}}$ Setup Time to Clock ↓	(60)	—	(45)	—
18	ThWT(Cf)	$\overline{\text{WAIT}}$ Hold Time after Clock ↓	—	0	—	0
19	TdC(M1f)	Clock ↑ to $\overline{\text{M1}}$ ↓ Delay	—	80	—	70
20	TdC(M1r)	Clock ↑ to $\overline{\text{M1}}$ ↑ Delay	—	80	—	70
21	TdCr(RFSHf)	Clock ↑ to $\overline{\text{RFSH}}$ ↓ Delay	—	110	—	95
22	TdC(RFSHr)	Clock ↑ to $\overline{\text{RFSH}}$ ↑ Delay	—	100	—	85
23	TdC(RDr)	Clock ↓ to $\overline{\text{RD}}$ ↑ Delay	—	70	—	60
24	TdCr(RDf)	Clock ↑ to $\overline{\text{RD}}$ ↓ Delay	—	70	—	60
25	TsD(Cf)	Data Setup to Clock ↓ during M_2, M_3, M_4 or M_5 Cycles	40	—	30	—
26	TdA(IORQf)	Address Stable prior to $\overline{\text{IORQ}}$ ↓	110*	—	75*	—
27	TdCr(IORQf)	Clock ↑ to $\overline{\text{IORQ}}$ ↓ Delay	—	65	—	55
28	TdCf(IORQr)	Clock ↓ to $\overline{\text{IORQ}}$ ↑ Delay	—	70	—	60
29	TdD(WRf)	Data Stable prior to $\overline{\text{WR}}$ ↓	25*	—	5*	—
30	TdCf(WRf)	Clock ↓ to $\overline{\text{WR}}$ ↓ Delay	—	70	—	60
31	TwWR	$\overline{\text{WR}}$ Pulse Width	135*	—	100*	—
32	TdCf(WRr)	Clock ↓ to $\overline{\text{WR}}$ ↑ Delay	—	70	—	60
33	TdD(WRf)	Data Stable prior to $\overline{\text{WR}}$ ↓	55*	—	55*	—
34	TdCr(WRf)	Clock ↑ to $\overline{\text{WR}}$ ↓ Delay	—	60	—	55
35	TdWRr(D)	Data Stable from $\overline{\text{WR}}$ ↑	30*	—	15*	—
36	TdCf(HALT)	Clock ↓ to $\overline{\text{HALT}}$ ↑ or ↓	—	260	—	225
37	TwNMI	$\overline{\text{NMI}}$ Pulse Width	70	—	60*	—
38	TsBUSREQ(Cr)	$\overline{\text{BUSREQ}}$ Setup Time to Clock ↑	50	—	40	—

*For clock periods other than the minimums shown in the table, calculate parameters using the expressions in the table on the following page.

†All timings assume equal loading on pins within 50 pF.

Timings are preliminary and subject to change.

AC Characteristics

Number	Symbol	Parameter	Z80B CPU Min	Z80B CPU Max	Z80H CPU† Min	Z80H CPU† Max
39	ThBUSREQ(Cr)	BUSREQ Hold Time after Clock ↑	0	—	0	—
40	TdCr(BUSACKf)	Clock ↑ to BUSACK ↓ Delay	—	90	—	80
41	TdCf(BUSACKr)	Clock ↓ to BUSACK ↑ Delay	—	90	—	80
42	TdCr(Dz)	Clock ↑ to Data Float Delay	—	80	—	70
43	TdCr(CTz)	Clock ↑ to Control Outputs Float Delay (MREQ, IORQ, RD, and WR)	—	70	—	60
44	TdCr(Az)	Clock ↑ to Address Float Delay	—	80	—	70
45	TdCTr(A)	Address Stable prior to MREQ ↑, IORQ ↑, RD ↑, and WR ↑	35*	— —	20*	—
46	TsRESET(Cr)	RESET to Clock ↑ Setup Time	60	—	45	—
47	ThRESET(Cr)	RESET to Clock ↑ Hold Time	—	0	—	0
48	TsINTf(Cr)	INT to Clock ↑ Setup Time	70	—	55	—
49	ThINTr(Cr)	INT to Clock ↑ Hold Time	—	0	—	0
50	TdM1f(IORQf)	M1 ↓ to IORQ ↓ Delay	35*	—	20*	—
51	TdCf(IORQf)	Clock ↓ to IORQ ↓ Delay	—	70	—	60
52	TdCf(IORQr)	Clock ↑ to IORQ ↑ Delay	—	70	—	60
53	TdCr(D)	Clock ↑ to Data Valid Delay	—	130	—	115

*For clock periods other than the minimums shown in the table, calculate parameters using the following expressions. Calculated values above assumed TrC = TfC = 20 ns.

† All timings assume equal loading on pins with 50 pF.

Timings are preliminary and subject to change.

Footnotes to AC Characteristics

Number	Symbol	Z80B	Z80H
1	TcC	TwCh + TwCl + TrC + TfC	TwCh + TwCl + TrC + TfC
2	TwCh	Although static by design, TwCh of greater than 200 μs is not guaranteed	Although static by design, TwCh of greater than 200 μs is not guaranteed
7	TdA(MR)	TwCh + TfC − 50	TwCh + TfC − 45
10	TwMRh	TwCh + TfC − 20	TwCh + TfC − 20
11	TwMRl	TcC − 30	TcC − 25
26	TdA(IR)	TcC − 55	TcC − 50
29	TdDO(WRm)	TcC − 140	TcC − 120
31	TwWR	TcC − 30	TcC − 25
33	TdDO(WRi)	TwCl + TrC − 140	TwCl + TrC − 120
35	TdWR(DO)	TwCl + TrC − 55	TwCl + TrC − 50
45	TdCT(A)	TwCl + TrC − 50	TwCl + TrC − 45
50	TdM1(IR)	2TcC + TwCh + TfC − 50	2TcC + TwCh + TfC − 45

*For clock periods other than the minimums shown in the table, calculate parameters using the expressions in the table on the following page.

†All timings assume equal loading on pins within 50 pF.

Timings are preliminary and subject to change.

Zilog Sales Offices

West

Sales & Technical Center
Zilog, Incorporated
1315 Dell Avenue
Campbell, CA 95008
Phone: (408) 370-8120
TWX: 910-338-7621

Sales & Technical Center
Zilog, Incorporated
18023 Sky Park Circle
Suite J
Irvine, CA 92714
Phone: (714) 549-2891
TWX: 910-595-2803

Sales & Technical Center
Zilog, Incorporated
15643 Sherman Way
Suite 430
Van Nuys, CA 91406
Phone: (213) 989-7485
TWX: 910-495-1765

Sales & Technical Center
Zilog, Incorporated
1750 112th Ave. N.E.
Suite D161
Bellevue, WA 98004
Phone: (206) 454-5597

Midwest

Sales & Technical Center
Zilog, Incorporated
951 North Plum Grove Road
Suite F
Schaumburg, IL 60195
Phone: (312) 885-8080
TWX: 910-291-1064

Sales & Technical Center
Zilog, Incorporated
28349 Chagrin Blvd.
Suite 109
Woodmere, OH 44122
Phone: (216) 831-7040
FAX: 216-831-2957

South

Sales & Technical Center
Zilog, Incorporated
4851 Keller Springs Road,
Suite 211
Dallas, TX 75248
Phone: (214) 931-9090
TWX: 910-860-5850

Zilog, Incorporated
7113 Burnet Rd.
Suite 207
Austin, TX 78757
Phone: (512) 453-3216

Zilog, Incorporated
9 Greenway Plaza
2400 Coastal Tower
Houston, TX 77046
Phone: (713) 840-5475

East

Sales & Technical Center
Zilog, Incorporated
Corporate Place
99 South Bedford St.
Burlington, MA 01803
Phone: (617) 273-4222
TWX: 710-332-1726

Sales & Technical Center
Zilog, Incorporated
240 Cedar Knolls Rd.
Cedar Knolls, NJ 07927
Phone: (201) 540-1671

Technical Center
Zilog, Incorporated
3300 Buckeye Rd.
Suite 401
Atlanta, GA 30341
Phone: (404) 451-8425

Sales & Technical Center
Zilog, Incorporated
1442 U.S. Hwy 19 South
Suite 135
Clearwater, FL 33516
Phone: (813) 535-5571

Zilog, Inc.
613-B Pitt St.
Cornwall, Ontario
Canada K6J 3R8
Phone: (613) 938-1121

Zilog, Incorporated
1700 N. Moore Street
Suite 1030
Arlington, VA 22209
Phone: (703) 243-7900

Zilog, Incorporated
1270 Avenue of the Americas
Eleventh Floor
New York, NY 10020
Phone: (212) 398-4497

United Kingdom

Zilog (U.K.) Limited
Zilog House
43-53 Moorbridge Road
Maidenhead
Berkshire, SL6 8PL England
Phone: 0628-39200
Telex: 848609

France

Zilog, Incorporated
Tour Europe
Cedex 7
92080 Paris La Defense
France
Phone: (1) 778-14-33
Telex: 611445F

West Germany

Zilog GmbH
Eschenstrasse 8
D-8028 TAUFKIRCHEN
Munich, West Germany
Phone: 89-612-6046
Telex: 529110 Zilog d.

Japan

Zilog, Japan K.K.
Konparu Bldg. 5F
2-8 Akasaka 4-Chome
Minato-Ku, Tokyo 107
Japan
Phone: (81) (03) 587-0528
Telex: 2422024 A/B: Zilog J

Zilog, Inc. 1315 Dell Ave., Campbell, California 95008 Telephone (408)370-8000 TWX 910-338-7621

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